//testbench

module msmachinetb;

reg inp, clk;

wire out;

msmachine uut(.inp(inp), .clk(clk), .out(out));

initial begin

$dumpfile("msmachine.vcd");

$dumpvars(1, msmachinetb);

clk=0;

forever #5 clk= ~clk;

end

initial begin

clk = 1'b0;

inp = 0;

#10

inp = 0;

#10;

inp = 1;

#10;

$finish;

end

endmodule

//design

module msmachine (

input inp, clk, rst,

output reg out

);

reg state;

parameter A=0, B=1;

always @(posedge clk or posedge rst) begin

if (rst)

state <= B;

else

state <= (inp == 0) ? A : B;

end

always @(posedge clk or posedge rst) begin

if (rst)

out <= 0;

else begin

case (state)

A: out <= (inp == 0) ? 1 : 0;

B: out <= (inp == 0) ? 0 : 1;

default: out <= 0;

endcase

end

end

endmodule